UN603

Silicon PNP epitaxial planer transistor

For DC-DC converter

Features

- Two elements incorporated into one package.
- Reduction of the mounting area and assembly cost by one half.
- Automatic mounting possible through 12mm wide emboss-taping supply.

Basic Part Number of Element

• $2SA1674 \times 2$ elements

Absolute Maximum Ratings (Ta=25°C)

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Parameter	Symbol	Ratings	Unit	
Collector to base voltage	V _{CBO}	-80	V	
Collector to emitter voltage	V _{CEO}	-80	V	
Emitter to base voltage	V_{EBO}	-5	V	
Collector current	$I_{\rm C}$	-1	A	
Peak collector current	I_{CP}	-1.5	A	
Total power dissipation	P _T *1	1	W	
Junction temperature	$T_{\rm j}$	150	°C	
Storage temperature	T _{stg}	-55 to +150	°C	

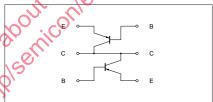
^{*1} Printed circuit board: Copper foil area of 4cm² or more and thickness of 1.7mm for the collector portion.

Electrical Characteristics (Ta=25°C)

Unit: mm

Marking Symbol: 60

Internal Connection



Parameter	Symbol	Conditions	min	typ	max	Unit
Collector to base voltage	V _{CBO}	$I_C = 10 \mu A, I_E = 0$	-80			V
Collector to emitter voltage	V _{CEO}	$I_C = -1 \mathrm{mA}, I_B = 0$	-80			V
Emitter to base voltage	V _{EBO}	$I_{\rm E} = -10\mu A, I_{\rm C} = 0$	-5			V
Collector cutoff current	I_{CBO}	$V_{CB} = -40V, I_E = 0$			-0.1	μA
Forward current transfer ratio	h _{FE1}	$V_{CE} = -2V, I_{C} = -100mA*$	120		340	
	h _{FE2}	$V_{CE} = -2V, I_{C} = -500 \text{mA*}$	60			
Collector to emitter saturation voltage	V _{CE(sat)}	$I_C = -500 \text{mA}, I_B = -50 \text{mA}*$		- 0.2	- 0.3	V
Base to emitter saturation voltage	V _{BE(sat)}	$I_C = -500 \text{mA}, I_B = -50 \text{mA}*$		- 0.85	-1.2	V
Transition frequency	f_T	$V_{CB} = -10V$, $I_E = 50$ mA, $f = 200$ MHz		120		MHz
Collector output capacitance	C _{ob}	$V_{CB} = -10V, I_E = 0, f = 1MHz$		15	30	pF

^{*} Pulse test

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